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10/605,502	10/03/2003	Yi-Tsung Cheng	HTCP0013USA	2501

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EXAMINER
BECK, ALEXANDER S

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
09/17/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/605,502	CHENG, YI-TSUNG	
	Examiner	Art Unit	
	Alexander S. Beck	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendment filed by the applicant on June 22, 2007, in response to the non-final Office action mailed on March 23, 2007, and in which: new claims 18-26 are added; and the rejections of the claims are traversed. Claims 1-26 are currently pending in U.S. Patent Application No. 10/605,502 and an Office action on the merits follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7 and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over an English translation of JP Patent No. 62-251917 to Nakazawa et al. (hereinafter "Nakazawa") in view of U.S. Patent No. 4,414,538 to Schnizlein (hereinafter "Schnizlein").

As to claim 1, Nakazawa discloses a keyboard comprising a key module (10) comprising at least one key cell with an output end being selectively connected to one of a first voltage and a second voltage. (Nakazawa at pp. 5-6, 8.) A detect circuit (20) is electrically connected to the output end of the key cell for generating a control signal whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage. (Nakazawa at pp. 5-6, 8.) A processor (21) is electrically connected to the detect circuit. (Nakazawa at pp. 6-8.)

Nakazawa does not disclose expressly a parallel-to-serial register electrically connected to the output end of the key module; and the processor electrically connected to the parallel-to-serial register and the detect circuit controlling the parallel-to-serial register according to the control signal. However, the use of a parallel-to-serial register in keyboard applications is old and well known in the art for converting parallel output data into serial output data for transmission to additional processing equipment. For example, Schnizlein discloses a keyboard comprising a parallel-to-serial register (64) electrically connected to the output end of a key module, wherein the parallel-to-serial register is operative in response to a signal representative of a depressed key cell. (Schnizlein at col. 4 ll. 2-19.)

All of the component parts are known in Nakazawa and Schnizlein. The only difference is the combination of the "old elements" into a single keyboard. Thus, it would have been obvious to a person of ordinary skill in the art to implement the parallel-to-serial register taught by Schnizlein into the keyboard of Nakazawa, since a parallel-to-serial register could be used in combination with a standard keyboard to achieve the predictable result of converting parallel output data into serial output data for transmission to additional processing equipment. As such, the modified embodiment comprising the processor of Nakazawa electrically connected to the parallel-to-serial register, and the detect circuit of Nakazawa controlling the parallel-to-serial register according to the control signal, wherein the control signal is generated whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage.

As to claim 7, most of the claimed limitations have already been discussed and met by Nakazawa and Schnizlein, as detailed in the above paragraphs with respect to claim 1, with the

exception of "detecting a transient voltage at the moment when the key cell is pressed or released and then generating a control signal". However, Nakazawa discloses the detect circuit (20) detecting a transient voltage at the moment when the key cell is pressed or released, resulting in a potential decrease from +5 V to 0 V, and then generating a control signal. (Nakazawa at pp. 5-6, 8.)

As to claim 16, all of the claimed limitations have already been discussed and met by Nakazawa and Schnizlein, as detailed in the above paragraphs with respect to claim 1. For example, Nakazawa as modified by Schnizlein teaches/suggests a parallel-to-serial register for inputting data from the output end when the key cell is pressed or released; and a processor for controlling the parallel-to-serial register and reading the input data therein only upon reception of the control signal. (Nakazawa at pp. 6-8.) (Schnizlein at col. 4 ll. 2-19.)

As to claim 17, all of the claimed limitations have already been discussed and met by Nakazawa and Schnizlein, as detailed in the above paragraphs with respect to claims 1 and 7.

As to claim 18-21, Nakazawa as modified by Schnizlein teaches/suggest a plurality of key cells each having an output end connected to one of the first voltage and the second voltage; and the parallel-to-serial register electrically connected to the output end of each of the key cells in the key module for reading a parallel input being the voltage at the output end of all the key cells and converting the parallel input into a serial representation for output to the processor. (Nakazawa at pp. 6-8.) (Schnizlein at col. 4 ll. 2-19.)

As to claim 22, Nakazawa as modified by Schnizlein teaches/suggests wherein the detect circuit (20) is further for asserting the control signal only while detecting a transient voltage being less than a reference voltage (e.g. going from 5v to 0v), the transient voltage corresponding

to a change in voltage at the output end of the key cell and being a voltage spike that occurs at the moment the output end of the key cell becomes connected to the other of the second and the first voltage. (Nakazawa at p. 6.) Nakazawa does not disclose expressly wherein the detect circuit detects a transient voltage being greater than a reference voltage (e.g. going from 0v to 5v). However, at the time the invention was made it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify Nakazawa and Schnizlein such that the detect circuit detects a transient voltage being greater than a reference voltage (e.g. going from 0v to 5v) because applicant has not disclosed that this limitation provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with detecting a transient voltage being less than a reference voltage (e.g. going from 5v to 0v) because either method is capable of determining whether a key depression occurs.

4. Claims 2, 3 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa and Schnizlein as applied to claims 1, 7 and 16-22 above, and further in view of U.S. Patent No. 4,027,306 to Hackmeister (hereinafter "Hackmeister").

As to claims 2, 3, 8-10, note the above discussion of Nakazawa and Schnizlein. Neither Nakazawa nor Schnizlein disclose expressly wherein the detect circuit comprises at least one capacitor corresponding to and electrically connected to the at least one key cell within the key module and an amplifying circuit electrically connected to the capacitor for amplifying the voltage in the capacitor. However, the use of a capacitive element for storing a voltage and an amplifier to amplify the voltage is old and well known in the art during the pre-processing steps of an electronic device for an improvement in processing. Hackmeister discloses a touch-

responsive circuit and data input terminal comprising: a key module (11) comprising at least one key cell (13') and a detect circuit (12) comprising at least one capacitor (26) corresponding to each key cell within the key module and an amplifying circuit (28) for amplifying the voltage in the capacitor. (Hackmeister at col. 3, ln. 64 – col. 4, ln. 21.)

All of the component parts are known in Nakazawa, Schnizlein and Hackmeister. The only difference is the combination of the "old elements" into a single keyboard. Thus, it would have been obvious to a person of ordinary skill in the art to implement the at least one capacitor and amplifying circuit taught by Hackmeister into the keyboard taught by Nakazawa and Schnizlein, since a capacitor and amplifying circuit could be used in combination with a standard keyboard to achieve the predictable result of conducting a voltage indicative of a depression of the key cell followed by the sufficient amplification of the conducted voltage by an amplifier to a level applicable for use during processing.

Moreover, Nakazawa and Schnizlein as modified by Hackmeister teaches/suggests wherein the detect circuit further comprises a comparator electrically connected to the capacitor for generating the control signal by comparing the transient voltage with a reference voltage, wherein this limitation is inherently suggested in the comparison of a depressed voltage, represented by 0v, with a non-depressed voltage, represented by +5v, prior to the generation of signal h to identify the depression of a key. (Nakazawa at pp. 5-6, 8.)

5. Claims 4-6, 11-15 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa, Schnizlein and Hackmeister as applied to claims 1-3, 7-10 and 16-22 above, and further in view of U.S. Patent No. 6,265,993 to Johnson (hereinafter "Johnson").

As to claims 4, 5, 11 and 12, note the above discussion of Nakazawa, Schnizlein and Hackmeister. Nakazawa as modified by Schnizlein and Hackmeister teaches/suggests the comparator electrically connected to the amplifying circuit, for comparing whether the voltage of the output end of the amplifying circuit is in a predetermined range and generating the control signal accordingly. (Nakazawa at pp. 5-6, 8.) Neither Nakazawa, Schnizlein nor Hackmeister disclose expressly a positive comparator and a negative comparator for generating the control signal when the voltage output from the output end of the amplifying circuit exceeds a positive reference voltage, and a negative comparator for generating the control signal when the voltage output from the output end of the amplifying circuit is lower than a negative reference voltage. Johnson discloses a keyboard comprising a pair of detection means (72/74) for allowing the keyboard to separately identify positive and negative key group input signals and thereby distinguish key presses from key releases. (Johnson at col. 7, ll. 56-65.)

All of the component parts are known in Nakazawa, Schnizlein and Hackmeister. The only difference is the combination of the "old elements" into a single keyboard. Thus, it would have been obvious to a person of ordinary skill in the art to implement the positive comparator and the negative comparator taught by Hackmeister into the keyboard taught of Nakazawa, Schnizlein and Hackmeister, since a positive comparator and a negative comparator could be used in combination with a standard keyboard to achieve the predictable result of allowing the keyboard to separately identify positive and negative key group input signals and thereby distinguish key presses from key releases.

As to claims 6 and 14, note the above discussion of Nakazawa, Schnizlein, Hackmeister and Johnson. Neither Nakazawa, Schnizlein, Hackmeister nor Johnson disclose expressly

wherein the detect circuit comprises an OR gate for performing the step of determining whether a control signal is to be output. However, the examiner takes Official Notice that the use of an OR gate to perform a simple Boolean expression such as determining whether any of a plurality of inputs are high (e.g. determining which keys are within a predetermined range so as to output a control signal) is old and well known in the art.

Thus, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the teachings of Nakazawa, Schnizlein, Hackmeister and Johnson such that the step of determining whether a control signal is to be output was performed by an OR gate. The suggestion/motivation for doing so would have been because OR gates are very common in the art, readily available, and cheap to manufacture. Moreover, an OR gate can be used in combination with a standard keyboard receiving a plurality of inputs for the predictable results of determining whether there are any keys within a predetermined range so as to output a control signal.

As to claims 13 and 15, Nakazawa as modified by Schnizlein, Hackmeister and Johnson teaches/suggests the detect circuit having an amplifier electrically connecting the capacitor and the set of comparators for amplifying the transient voltage. (Hackmeister at col. 3, ln. 63 – col. 4, ln. 21.)

As to claims 23-25, note the above discussion with respect to claims 4, 5, 11 and 12. Nakazawa as modified by Schnizlein, Hackmeister and Johnson teaches/suggests wherein the detect circuit is further for asserting the control signal only while detecting the transient voltage being greater than a reference voltage, the transient voltage being a voltage spike that occurs at

the moment the key cell is pressed and at the moment the key cell is released. (Nakazawa at pp. 6-8.) (Johnson at col. 7, ll. 56-65.)

6. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa in view of Schnizlein, Hackmeister, Johnson and U.S. Patent No. 4,405,918 to Wall et al. (hereinafter "Wall").

As to claim 26, most of the claim limitations have already been discussed and met by Nakazawa, Schnizlein, Hackmeister and Johnson as applied to claims 1-15 above, with the exception of the first comparator having a positive input terminal for receiving a key voltage and having a negative input terminal coupled to a positive reference voltage, and a second comparator having a negative input terminal for receiving a key voltage and having a positive input terminal coupled to a negative reference voltage. As discussed above, Johnson discloses a keyboard comprising a positive comparator and a negative comparator (72/74) for allowing the keyboard to separately identify positive and negative key group input signals and thereby distinguish key presses from key releases. (Johnson at col. 7, ll. 56-65.) However, none of the applied references disclose expressly the positive/negative input terminal connections as claimed.

Wall discloses a positive comparator for determining key presses and having a positive input terminal for receiving a key voltage and having a negative input terminal coupled to a positive reference voltage. (Wall at Figure 5.) Because both Johnson and Wall teach positive comparators for detecting a key depression, it would have been obvious to one skilled in the art to substitute one positive comparator for the other to achieve the predictable result of detecting a key depression based on a positive key voltage. Although Wall does not disclose expressly a

negative comparator, it would have been within the purview of one having ordinary skill in the art to substitute the negative comparator of Johnson with a slightly modified comparator of Wall, having a negative input terminal for receiving a key voltage and having a positive input terminal coupled to a negative reference voltage, in order to achieve the predictable result of detecting a key release based on a negative key voltage.

Response to Arguments

7. Applicant's arguments filed June 22, 2007, have been fully considered but they are not persuasive. It is believed that all of applicant's arguments have been addressed in the rejection paragraphs and explanations above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander S. Beck whose telephone number is (571) 272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

asb
September 3, 2007

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER